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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,981	10/20/2003	Beom-jun Jin	5649-1135	8976

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EXAMINER	
KARIMY, MOHAMMAD TIMOR	
ART UNIT	PAPER NUMBER
2815	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,981	JIN, BEOM-JUN	
	Examiner	Art Unit	
	MOHAMMAD Timor KARIMY	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 10 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claim 1 recites the limitation "a sidewall of the hole" in lines 3, 5 & 8. It is not clear as to where in the drawings (Applicant's Fig. 7-8) the sidewall is positioned. In applicant's Fig. 7, is the sidewall directly contacting silicon oxide layer 452a or the sidewall is directly contacting silicon nitride layer 454a? The same ambiguity surrounding "sidewall" exists in applicant's Fig. 8. This limitation must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a **sidewall** of the hole" in lines 3, 5 & 8. It is not clear as to where in the drawings (Applicant's Fig. 7-8) the sidewall is positioned. In applicant's Fig. 7, is the sidewall directly contacting silicon oxide layer 452a or the sidewall is directly contacting silicon nitride layer 454a? The same ambiguity surrounding "sidewall" exists in applicant's Fig. 8. In view of the lack of clarity surrounding "a sidewall of the contact hole", it is not clear as to which reference numeral (452a or 454a) refers to the limitations "a first spacer" and "a second spacer". Clarification/correction is required.

Claim 10 recites the limitation "**the** sidewall of the contact hole" in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 also recites the limitation "gate line **patterns**" in line 4. It is not clear as to what elements within a gate structure this limitation include. Clarification is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5 & 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koga et al. (US Patent 6,649,500 B2) in view of Igarashi et al. (US Patent 6,838,732 B2).

With regard to claim 1, Koga teaches in figure 10(d) an integrated circuit device comprising:

a conductive contact 213a in a hole 212 in an interlevel dielectric layer;

a first spacer 207 having a first dielectric constant on a side wall of the hole; and

a second spacer 209 having a second dielectric constant located between the first spacer and the side wall of the hole, wherein the first dielectric constant is less than the second dielectric constant.

However, Koga does not explicitly teach a contact pad connected to the conductive contact. Nonetheless, Igarashi teaches in figure 16, wherein a silicide contact pad 105 is positioned to make an ohmic contact with a diffusion layer 104 underneath. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Koga by using a silicide contact pad as taught by Igarashi in the interest of an ohmic contact with the diffusion layer 208 underneath. The motivation for using ohmic contact is known in the art to be low-resistance and stable

contacts that improve the performance and reliability of integrated circuit devices. Therefore, Koga and Igarashi are combinable. Moreover, Igarashi's contact pad 115 covers the entirety of the surface underneath the conductive contact 106, therefore, once used in Koga's device, Koga's first spacer will extend to contact the silicide contact pad, and Koga's second spacer will not contact the silicide contact pad.

With respect to claim 2, Koga teaches in figure 10(d) the integrated circuit device according to claim 1, wherein the first spacer 207 comprises silicon oxide and the second spacer 209 comprises silicon nitride.

With respect to claim 3, Koga teaches in figure 10(d) the integrated circuit device according to claim 1, wherein the thickness of the first spacer is in about 50 A° (column 6 line 52).

With respect to claim 5, Koga teaches in figure 10(d) the integrated circuit device according to claim 1, further comprising:

a conductive line 204 in the interlevel dielectric layer adjacent to the first spacer opposite the conductive contact.

With respect to claim 28, Koga teaches in figure 10(d) the integrated circuit device according to claim 5, wherein the conductive line comprises a gate line pattern.

With respect to claim 29, Koga teaches in figure 10(d) the integrated circuit device according to claim 5, wherein the conductive line comprises a bit line pattern.

With respect to claim 30, Koga teaches in figure 10(d) the integrated circuit device according to claim 5, wherein the conductive line comprises an interconnection line pattern.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koga et al. (US Patent 6,649,500 B2) and Igarashi et al. (US Patent 6,838,732 B2) as applied to claims 1-3, and in further view of Yokoyama (US Patent 6,703,715 B2).

With respect to claim 4, Koga does not explicitly teach a thickness of between 10 A° and 300 A° for the second spacer. Koga, however, teaches a thickness of 500 A° for the second spacer. Nonetheless, these claimed dimensions are considered obvious to one of ordinary skill in the art in view of Koga. For instance, Yokoyama teaches in column 7 lines 60-51 a thickness of about 200 A° for a spacer. One of ordinary skill in the art is motivated to form device features within and about 10 A° and 300 A° to provide proper isolation as well as allow proper device operation. As such, it would have been obvious to use the aforementioned range of about 10 A° and 300 A°.

These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir.1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955)(selection of optimum ranges within prior art general conditions is obvious).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koga et al. (US Patent 6,649,500 B2) and Igarashi et al. (US Patent 6,838,732 B2), and in further view of Yokoyama (US Patent 6,703,715 B2).

With respect to claim 10, Koga teaches in figure 10(d) an integrated circuit device comprising:

an integrated circuit substrate (column 14, lines 32-33) in which source/drain regions 208 are formed;

a first interlevel dielectric layer 210 which is formed on the integrated circuit substrate;

gate line patterns 203 which are formed in the first interlevel dielectric layer;

first contact spacers 207 which are formed along the side walls of the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers 209 which formed of silicon nitride and formed on the first contact spacers; and

contact plugs 213a which are present in the contact holes between the second contact spacers.

However, Koga does not explicitly teach contact pads between adjacent gate line patterns and connected to the source/drain regions. Nonetheless, Igarashi teaches in figure 16, wherein a silicide contact pad 105 is positioned to make an ohmic contact with a diffusion layer 104 underneath. At the time of the invention, it would have been

obvious to a person of ordinary skill in the art to modify Koga by using a silicide contact pad as taught by Igarashi in the interest of an ohmic contact with the diffusion layer 208 underneath. The motivation for using ohmic contact is known in the art to be low-resistance and stable contacts that improve the performance and reliability of integrated circuit devices. Therefore, Koga and Igarashi are combinable.

Moreover, Koga does not explicitly teach a second interlevel dielectric layer on the first interlevel dielectric layer having a via hole. Nonetheless, the use of stacked interlevel dielectric layers is common in the semiconductor metallization structures. For instance, Yokoyama teaches in figure 5 interlevel dielectric layers 30 & 34a-b to provide insulation between neighboring elements. Moreover, the interlevel dielectric layers have via holes for electrical connection between the various levels. As such, the use of a second and/or third interlevel dielectric layers having contact holes is obvious to a person of ordinary skill in the art.

Response to Arguments

8. Applicant's arguments with respect to claims 1-5, 10 & 28-30 have been considered but are not persuasive. Claim 1 contains limitations that are ambiguous (please see *35 USC § 112* rejections above), and there also seems to be a discrepancy between the drawings (applicant's Fig. 7-8) and the claim limitations. It is unclear as to which reference numeral refers to “a first spacer" and “a second spacer”. Also, it is not clear as to where the limitation "sidewall of the contact hole" is. In other words, which one of the spacers (452a or 454a) directly contacts the sidewall.

As for applicant's argument regarding the motivation for a silicide ohmic contact, the advantages of an ohmic contact is well-known in the art which is low-contact resistance and stable contacts that results to an improved and reliable integrated circuit device. Furthermore, examiner maintains that the prior arts teach the gate patterns (203 & 204) that are in an interlevel dielectric layer 210. Also, as indicated in the claim 10 rejection, the use of stacked interlevel dielectric layers are commonly used in the art (see Yokoyama's Fig. 5), and their usage is obvious to a person of ordinary skill in the art. Moreover, the prior arts in combination teach the use of an ohmic contact to a diffusion region between adjacent gate structures. Contrary to applicant's argument, the ohmic contact as taught by Ingrashi, once employed in Kog'a device, and the contact plug 213 (see Koga's Fig. 10d) will both be located **in** an interlevel dielectric layer 210.

Therefore, the applicant's arguments are not persuasive.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (US Patent No. 6,383,882) and Cho et al. (US Patent 6,770,927 B2) discuss the use of spacers, gate patterns and interconnect structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad Timor Karimy whose telephone number is 571-272-9006. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mtk

/Eugene Lee/

Primary Examiner, Art Unit 2815